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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re the Application of: **MARUYAMA, et al.**

Group Art Unit: **2815**

Serial No.: **09/577,932**

Examiner: **Chris Chu**

Filed: **May 25, 2000**

P.T.O. Confirmation No.: 4823

**FOR: SEMICONDUCTOR DEVICE HAVING AN ALIGNMENT MARK FORMED BY THE SAME MATERIAL WITH A METAL POST**

**AMENDMENT TRANSMITTAL**

Commissioner for Patents  
Washington, D.C. 20231

January 22, 2003

Sir:

Transmitted herewith is an Amendment in the above-identified application.

The fee has been calculated as shown below:

	CLAIMS AS AMENDED						
	Claims Remaining After Amendment	Highest Number Previously Paid For		Present Extra	Small Entity	Large Entity	Additional Fee
Total Claims	15	20	=	0	X \$9	X \$18	0.00
Independent Claims	9	8	=	1	X \$42	X \$84	84.00
First Presentation of Multiple Dependent Claims					\$140	280	
TOTAL FEES ENCLOSED:							84.00

**XX** Enclosed please find our check in the amount of \$84.00 for the additional claims fee in connection with this amendment.

**XX** The Commissioner is hereby authorized to charge payment for any additional fees associated with this communication or credit any overpayment to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP



Michael N. Lau  
Attorney for Applicant  
Reg. No. 39,479

MNL/alw

Atty. Docket No. **000663**  
Suite 1000, 1725 K Street, N.W.  
Washington, D.C. 20006  
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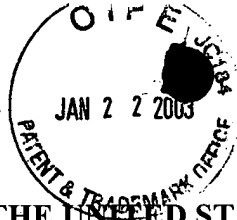


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Enclosures: Response under 37 CFR 1.116



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**RESPONSE UNDER 37 CFR §1.116**

**- EXPEDITED RESPONSE -**

**GROUP ART UNIT 2815**

**BOX AF**

Commissioner for Patents  
Washington, D.C. 20231

January 22, 2003

Sir:

In response to the Office Action dated **October 22, 2002**, please amend the above-identified application as follows:

**IN THE CLAIMS:**

Please amend claims 1, 4, 13 and 14 as indicated below:

1. (Thrice Amended) A semiconductor device comprising:
- a semiconductor element having a plurality of electrodes;
  - a redistribution layer having a plurality of electrode pads and conductive patterns connecting the electrodes of the semiconductor element to the respective electrode pads;
  - a plurality of metal posts each with a first shape and a first size formed on the electrode pads of the redistribution layer, the metal posts being configured to be provided with external connection

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